



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/087,672	02/27/2002	Jered Donald Aasheim	MS1-1026US	6395

22801 7590 06/13/2006

LEE & HAYES PLLC  
421 W RIVERSIDE AVENUE SUITE 500  
SPOKANE, WA 99201

EXAMINER
----------

PATEL, HETUL B

ART UNIT	PAPER NUMBER
----------	--------------

2186

DATE MAILED: 06/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/087,672	AASHEIM ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Hetul Patel	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 21 April 2006.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-44 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-44 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                                   | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)               | Paper No(s)/Mail Date. _____  |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>04/21/2006</u> .  | 6) <input type="checkbox"/> Other: _____                                    |

### DETAILED ACTION

1. This action is responsive to communication filed on April 21, 2006. This amendment has been entered and carefully considered. Claims 1-44 are again presented for examination.
2. Applicant's arguments filed on April 21, 2006 have been fully considered but they are not deemed to be persuasive.
3. The IDS filed on 04/21/2006 has been considered.
4. This office action is made non-final since new grounds of rejection are presented.

### ***Claim Rejections - 35 USC § 101***

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. Claims 1-8 and 41-44 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claim 1 is not limited to tangible embodiments. In view of applicants' disclosure, specification page 31, line 17 – page 32, line 17, the computer-readable media is not limited to tangible embodiments, instead being defined as including both tangible embodiments (e.g., computer storage media as defined on page 32, lines 1-7) and intangible embodiments (e.g. modulated data signals as defined on page 32, lines 12-17). As such, the claim is not limited to statutory subject matter and is therefore non-statutory."

### DETAILED ACTION

1. This action is responsive to communication filed on April 21, 2006. This amendment has been entered and carefully considered. Claims 1-44 are again presented for examination.
2. Applicant's arguments filed on April 21, 2006 have been fully considered but they are not deemed to be persuasive.
3. This office action is made non-final since new grounds of rejection are presented.

### ***Claim Rejections - 35 USC § 101***

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claims 1-8 and 41-44 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claim 1 is not limited to tangible embodiments. In view of applicants' disclosure, specification page 31, line 17 – page 32, line 17, the computer-readable media is not limited to tangible embodiments, instead being defined as including both tangible embodiments (e.g., computer storage media as defined on page 32, lines 1-7) and intangible embodiments (e.g. modulated data signals as defined on page 32, lines 12-17). As such, the claim is not limited to statutory subject matter and is therefore non-statutory."

Claims 2-8 are also rejected based on the same rational as they depend upon the rejected claim 1. Claims 41-44 are also rejected based on the same rational as the rejection of claim 1, i.e. the computer-readable medium is not limited to tangible embodiments.

### ***Claim Rejections - 35 USC § 112***

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. As disclosed above, since claims 1-8 and 41-44 are including intangible embodiments, these claims are also rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 5-7, 9-11, 16-17, 22-25, 29, 31-33, 37, 39 and 40-44 are rejected under 35 U.S.C. 102(b) as being anticipated by Ban (USPN: 5,799,168).

As per claim 1, Ban teaches that one or more computer-readable media (the combination of flash array and standardized flash controller in Fig. 1) comprising a flash

memory driver (the standardized flash controller in Fig. 1; i.e. the group of interfaces/controllers, between the CPU and the flash memory) that is executable by a computer to interface between a file system and one or more flash memory media, the flash memory driver comprising: flash abstraction logic (i.e. the group of interfaces/controllers, between the CPU and the flash memory) and invocable by the file system to manage flash memory operations without regard to the type of the one or more flash memory media (e.g. see Col. 2, lines 36-38); and flash media logic (a simple discrete logic or interface) configured to interact with different types of the flash memory media (any flash chip); wherein the flash abstraction logic invokes the flash media logic to perform memory operations (generic commands) that are potentially performed in different ways depending on the type of the flash memory media (e.g. see the abstract, Col. 2, lines 36-48; Col. 4, lines 33-39, 61-65 and claim 2). The further limitation of the flash memory driver is having flash memory medium agnostic is also taught by Ban, i.e. Ban also teaches that the flash memory driver, i.e. the whole group of interfaces/controllers, between the CPU and the flash memory (e.g. see Fig. 2). Therefore, even though a unique controller is being placed on each individual flash chip, "the group of interfaces/controller" as a whole manages flash memory operations without regard to the type of the one or more flash memory media as being claimed. Ban also teaches that the flash driver (the standardized flash controller in Fig. 1) is located remotely from the flash memory medium (i.e. the flash array in Fig. 1) (e.g. see Fig. 1).

As per claims 5 and 6, Ban teaches the claimed invention as described above and furthermore, Ban teaches the flash memory driver, wherein one of the flash memory operations includes mapping status information associated with physical sectors of the flash memory medium for use by the file system, i.e. translating commands from/to physical sectors of the flash memory medium to/from commands for used in the file system (CPU) (e.g. see Col. 5, lines 29-37).

As per claim 7, Ban teaches the claimed invention as described above and furthermore, Ban teaches the flash memory driver, wherein the flash medium logic (simple discrete logic) is a user programmable to read, write and erase data to and from the flash memory medium (e.g. see Col. 3, line 49 – Col. 4, line 13).

As per claim 17, Ban teaches the claimed invention as described above and furthermore, Ban teaches that the flash abstraction logic that is interface/controller, between the CPU and the flash memory, passes specific commands associated with certain types of flash memory media directly to the flash medium logic (a simple discrete logic or interface) for translation and further execution (e.g. see Col. 2, lines 36-48 and Fig. 1).

As per claims 23 and 29, Ban teaches a processing device that uses a flash memory medium for storage of data, comprising: a file system (the flash file system), configured to control data storage for the processing device (i.e. the CPU in Fig. 1) (e.g. see Col. 2, lines 17-23); flash media logic (a simple discrete logic or interface which comprises the command register) configured to perform physical sector operations to a flash memory medium based on physical sector commands, wherein the flash medium

Art Unit: 2186

logic comprises a set of programmable entry points that can be implemented by a user to interface with the type of flash memory medium selected (e.g. see Col. 3, lines 15-24); and flash abstraction logic that is interface/controller, between the CPU and the flash memory, configured to maintain flash memory requirements, which are common to a plurality of different flash memory media, that are necessary to operate the flash memory medium (e.g. see Col. 2, lines 36-48 and Fig. 1).

As per claim 40, Ban teaches the claimed invention as described above and furthermore, Ban teaches that the method further comprises receiving read and write commands from a file system that is inherently embedded in the controller taught by Ban (e.g. see Col. 1, lines 35-39 and Col. 2, lines 40-44).

As per claim 41, Ban teaches the claimed invention as described above and furthermore, Ban teaches that one or more computer-readable media (the combination of flash array and standardized flash controller in Fig. 1) comprising computer-executable instructions (commands stored in the command register) that, when executed, perform the method as taught by Ban (e.g. see Col. 3, lines 15-24 and Fig. 1).

As per claims 9, 18, 25 and 42-43, see argument with respect to the rejection of claim 1. Claims 9, 18, 25 and 42-43 are rejected based on the same rationale as the rejection of claim 1.

As per claims 11, 31 and 37, see argument with respect to the rejection of claim 6. Claims 11, 31 and 37 are rejected based on the same rationale as the rejection of claim 6.



As per claims 10, 22, 32, 39 and 44, see argument with respect to the rejection of claim 7. Claims 10, 22, 32, 39 and 44 are rejected based on the same rationale as the rejection of claim 7.

As per claim 16, see argument with respect to the rejection of claims 1 and 7. Claim 16 is rejected based on the same rationale as the rejection of claims 1 and 7.

As per claim 24, see argument with respect to the rejection of claim 17. Claim 24 is rejected based on the same rationale as the rejection of claim 17.

As per claim 33, see argument with respect to the rejection of claims 16 and 17. Claim 33 is rejected based on the same rationale as the rejection of claims 16 and 17.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 2, 12, 20, 27 and 35 rejected under 35 U.S.C. 103(a) as being unpatentable over Ban in view of Bruce et al. (USPN: 6,000,006) hereinafter, Bruce.

As per claim 2, Ban teaches the claimed invention as described above.

However, Ban failed to teach that one of the flash memory operations includes performing wear-leveling operations associated with the flash memory medium. Bruce, on the other hand, teaches that the benefits of using a unified re-mapping and wear-leveling table overcome the disadvantages of the larger granularity of block re-

mapping. As flash-memory sizes increase, the relative loss from block rather than page re-mapping decreases (e.g. see Col. 10, lines 7-15). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement the teachings of Bruce in the flash memory driver taught by Ban to recognize the benefits as stated above.

Claims 12, 20, 27 and 35 are rejected based on the same rationale as the rejection of claim 2.

8. Claims 3-4, 13-14, 19, 21, 26, 28, 34 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ban in view of Martwick (USPN: 6,493,807).

As per claims 3 and 4, Ban teaches the claimed invention as described above. However, Ban failed to teach that one of the flash memory operations includes maintaining data integrity of the flash memory medium and handling recovery of data associated with the flash memory medium after a power-failure. Martwick, on the other hand, teaches the method for updating the flash blocks so the data integrity gets maintained and the data can be recovered upon a power failure (e.g. see Col. 3, lines 37-39). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement the method of updating the flash blocks as taught by Martwick in the Ban's flash memory driver to recognize the benefits as stated above.

Claims 13-14, 19, 21, 26, 28, 34 and 36 are rejected based on the same rationale as the rejection of claims 3 and 4.

Art Unit: 2186

9. Claims 1, 5-7, 9-11, 16-17, 22-25, 29, 31-33, 37, 39 and 40-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ban (USPN: 5,799,168) in view of Hall (USPN: 6,253,281).

As per claim 1, Ban teaches that one or more computer-readable media (the combination of flash array and standardized flash controller in Fig. 1) comprising a flash memory driver (the standardized flash controller in Fig. 1) that is executable by a computer to interface between a file system and one or more flash memory media, the flash memory driver comprising: flash abstraction logic (i.e. the group of interfaces/controllers, between the CPU and the flash memory) that is invocable by the file system to manage flash memory operations (e.g. see Col. 2, lines 36-38); and flash media logic (a simple discrete logic or interface); wherein the flash abstraction logic invokes the flash media logic to perform memory operations (generic commands (e.g. see the abstract, Col. 2, lines 36-48; Col. 4, lines 33-39, 61-65 and claim 2).

Examiner is totally disagreed but just for the sake of argument, even if Ban fails to teach (a) the flash abstraction logic manages flash memory operations without regard to the type of the one or more flash memory media; (b) the flash media logic configured to interact with different types of the flash memory media; and (c) the flash abstraction logic invokes the flash media logic to perform memory operations that are potentially performed in different ways depending on the type of the flash memory media, Hall teaches these limitations. Hall teaches that the flash abstraction logic (i.e. the code in the system controller 1 in Fig. 1) manages flash memory operations without regard to the type of the one or more flash memory media (i.e. 22 in Fig. 1), i.e. the flash memory

Art Unit: 2186

driver is flash memory medium agnostic. Furthermore, Hall teaches the flash media logic (i.e. the system controller 1 in Fig. 1) that is configured to interact with different types of the flash memory media; and the flash abstraction logic invokes the flash media logic to perform memory operations that are potentially performed in different ways depending on the type of the flash memory media (e.g. see Col. 5, lines 31-48). Hall also teaches that the flash driver (i.e. the code in the system controller 1 in Fig. 1) is located remotely from the flash memory medium (i.e. 22 in Fig. 1) (e.g. see Fig. 1). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement the teachings of Hall in the flash memory driver taught by Ban. In doing so, it will be appreciated by those skilled in the art that FLASH memories produced by different manufacturers require different operations to erase and/or write data to them and these sequences are stored for a number of different memories within the microcontroller ROM. Thus the disc drive manufacturer is not confined to a single FLASH memory type and the micro controller does not have to be reprogrammed if a different type of FLASH memory is used.

As per claims 5 and 6, the combination of Ban and Hall teaches the claimed invention as described above and furthermore, Ban teaches the flash memory driver, wherein one of the flash memory operations includes mapping status information associated with physical sectors of the flash memory medium for use by the file system, i.e. translating commands from/to physical sectors of the flash memory medium to/from commands for used in the file system (CPU) (e.g. see Col. 5, lines 29-37).

As per claim 7, the combination of Ban and Hall teaches the claimed invention as described above and furthermore, Ban teaches the flash memory driver, wherein the flash medium logic (simple discrete logic) is a user programmable to read, write and erase data to and from the flash memory medium (e.g. see Col. 3, line 49 – Col. 4, line 13).

As per claim 17, the combination of Ban and Hall teaches the claimed invention as described above and furthermore, Ban teaches that the flash abstraction logic that is interface/controller, between the CPU and the flash memory, passes specific commands associated with certain types of flash memory media directly to the flash medium logic (a simple discrete logic or interface) for translation and further execution (e.g. see Col. 2, lines 36-48 and Fig. 1).

As per claims 23 and 29, the combination of Ban and Hall teaches a processing device that uses a flash memory medium for storage of data, comprising: a file system (the flash file system), configured to control data storage for the processing device (i.e. the CPU in Fig. 1) (e.g. see Col. 2, lines 17-23); flash media logic (a simple discrete logic or interface which comprises the command register) configured to perform physical sector operations to a flash memory medium based on physical sector commands, wherein the flash medium logic comprises a set of programmable entry points that can be implemented by a user to interface with the type of flash memory medium selected (e.g. see Col. 3, lines 15-24); and flash abstraction logic that is interface/controller, between the CPU and the flash memory, configured to maintain flash memory

Art Unit: 2186

requirements, which are common to a plurality of different flash memory media, that are necessary to operate the flash memory medium (e.g. see Col. 2, lines 36-48 and Fig. 1).

As per claim 40, the combination of Ban and Hall teaches the claimed invention as described above and furthermore, Ban teaches that the method further comprises receiving read and write commands from a file system that is inherently embedded in the controller taught by Ban (e.g. see Col. 1, lines 35-39 and Col. 2, lines 40-44).

As per claim 41, the combination of Ban and Hall teaches the claimed invention as described above and furthermore, Ban teaches that one or more computer-readable media (the combination of flash array and standardized flash controller in Fig. 1) comprising computer-executable instructions (commands stored in the command register) that, when executed, perform the method as taught by Ban (e.g. see Col. 3, lines 15-24 and Fig. 1).

As per claims 9, 18, 25 and 42-43, see argument with respect to the rejection of claim 1. Claims 9, 18, 25 and 42-43 are rejected based on the same rationale as the rejection of claim 1.

As per claims 11, 31 and 37, see argument with respect to the rejection of claim 6. Claims 11, 31 and 37 are rejected based on the same rationale as the rejection of claim 6.

As per claims 10, 22, 32, 39 and 44, see argument with respect to the rejection of claim 7. Claims 10, 22, 32, 39 and 44 are rejected based on the same rationale as the rejection of claim 7.

Art Unit: 2186

As per claim 16, see argument with respect to the rejection of claims 1 and 7.

Claim 16 is rejected based on the same rationale as the rejection of claims 1 and 7.

As per claim 24, see argument with respect to the rejection of claim 17. Claim 24 is rejected based on the same rationale as the rejection of claim 17.

As per claim 33, see argument with respect to the rejection of claims 16 and 17. Claim 33 is rejected based on the same rationale as the rejection of claims 16 and 17.

10. Claims 2, 12, 20, 27 and 35 rejected under 35 U.S.C. 103(a) as being unpatentable over Ban in view of Hall, further in view of Bruce et al. (USPN: 6,000,006) hereinafter, Bruce.

As per claim 2, the combination of Ban and Hall teaches the claimed invention as described above. However, both Ban and Hall failed to teach that one of the flash memory operations includes performing wear-leveling operations associated with the flash memory medium. Bruce, on the other hand, teaches that the benefits of using a unified re-mapping and wear-leveling table overcome the disadvantages of the larger granularity of block re-mapping. As flash-memory sizes increase, the relative loss from block rather than page re-mapping decreases (e.g. see Col. 10, lines 7-15).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement the teachings of Bruce in the flash memory driver taught by the combination of Ban and Hall to recognize the benefits as stated above.

Art Unit: 2186

Claims 12, 20, 27 and 35 are rejected based on the same rationale as the rejection of claim 2.

11. Claims 3-4, 13-14, 19, 21, 26, 28, 34 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ban in view of Hall, further in view of Martwick (USPN: 6,493,807).

As per claims 3 and 4, the combination of Ban and Hall teaches the claimed invention as described above. However, both Ban and Hall failed to teach that one of the flash memory operations includes maintaining data integrity of the flash memory medium and handling recovery of data associated with the flash memory medium after a power-failure. Martwick, on the other hand, teaches the method for updating the flash blocks so the data integrity gets maintained and the data can be recovered upon a power failure (e.g. see Col. 3, lines 37-39). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement the method of updating the flash blocks as taught by Martwick in the flash memory driver taught by the combination of Ban and Hall to recognize the benefits as stated above.

Claims 13-14, 19, 21, 26, 28, 34 and 36 are rejected based on the same rationale as the rejection of claims 3 and 4.

### ***Remarks***

12. As to the remark, Applicant asserted:



- (a) Ban fails to disclose “flash abstraction logic that is invokable by the file system to manage flash memory operations without regard to the type of the one or more flash memory media” as recited in claim 1 because the controllers used under Ban are flash chip specific, and cannot be used with other types of flash chips.
- (b) Ban fails to disclose “wherein the flash abstraction logic invokes the flash media logic to perform memory operations that are potentially performed in different ways depending on the type of the flash memory media”. Rather, under Ban the controllers are bound to a particular flash chip and thus are limited to performing memory operations specific to that flash chip.
- (c) Ban fails to disclose “the flash driver is located remote from the flash memory medium” as recited in claim 9.
- (d) Ban also fails to disclose or show both “user programmable flash medium logic, configured to read, write and erase data to and from flash memory medium” and “wherein the flash memory driver is flash memory medium agnostic”.
- (e) Ban fails to disclose the processing device of claims 23 and 33 since the flash media logic of claim 23 may be used with multiple, different flash media, while in Ban, multiple controllers would be needed to interface with multiple, different flash chips.

Examiner respectfully traverses Applicant's remark for the following reasons:

With respect to (a), in response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which

Art Unit: 2186

applicant relies (i.e., “the controllers used under Ban are flash chip specific, and cannot be used with other types of flash chips” and “controllers of Ban are ill-equipped to interact with different types of the flash memory chips”) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). The rejected claims states “flash abstraction logic that is invocable by the file system to manage flash memory operations without regard to the type of the one or more flash memory media and flash media logic configured to interact with different types of the flash memory media”. The flash abstraction logic is taught by Ban as the group of interfaces/controllers, between the CPU and the flash memories and the flash media logic is taught by Ban as the simple discrete logic/interface (e.g. see Col. 4, lines 33-39, 61-65 and Fig. 1).

Furthermore, as described above in the paragraph 9, just for the sake of argument, even if Ban fails to teach that the flash abstraction logic manages flash memory operations without regard to the type of the one or more flash memory media, Hall teaches that the flash abstraction logic (i.e. the code in the system controller 1 in Fig. 1) manages flash memory operations without regard to the type of the one or more flash memory media (i.e. 22 in Fig. 1), i.e. the flash memory driver is flash memory medium agnostic.

With respect to (b), as stated above the flash abstraction logic is equated with the group of interfaces/controllers of Ban between the CPU and the flash memories instead of one specific controller (e.g. see Col. 4, lines 33-39, 61-65 and Fig. 1). Therefore, Ban

does teach that the flash abstraction logic, i.e. the group of interfaces/controllers between the CPU and the flash memories, invokes the flash media logic to perform memory operations that are potentially performed in different ways depending on the type of the flash memory media, i.e. the specific controller would be used from the group of controllers depending on the type of the flash memory media.

With respect to (c), Ban clearly teaches that the flash driver (the standardized flash controller in Fig. 1) is located remotely from the flash memory medium (i.e. the flash array in Fig. 1) (e.g. see Fig. 1). Furthermore, as described above in the paragraph 9, just for the sake of argument, even if Ban fails to teach that the flash driver is located remote from the flash memory medium, Hall teaches that the flash driver (i.e. the code in the system controller 1 in Fig. 1) is located remotely from the flash memory medium (i.e. 22 in Fig. 1) (e.g. see Fig. 1).

With respect to (d), as recited in the rejection of claim 7 above, Ban clearly teaches the flash memory driver, wherein the flash medium logic is a user programmable to read, write and erase data to and from the flash memory medium (e.g. see Col. 3, line 49 – Col. 4, line 13). Furthermore, Ban also discloses that the flash driver (the standardized flash controller in Fig. 1) is located remotely from the flash memory medium (i.e. the flash array in Fig. 1) (e.g. see Fig. 1), therefore, the flash memory driver is flash memory medium agnostic.

With respect to (e), Ban does teach the processing device (i.e. CPU in Fig. 1) as claimed in claims 23 and 33. Examiner agreed with Applicant that in Ban, multiple controllers would be needed to interface with multiple, different flash chips. However,

Art Unit: 2186

the claimed flash abstraction logic is equated with the array/group of flash controllers taught by Ban and not any individual flash controller. Therefore, Ban does teach that the group of flash controllers may easily be used with multiple different flash media as claimed.

With respect to (d) and (e), Examiner respectfully disagrees with Applicant's argument because Ban clearly teaches about translating commands received from the CPU, i.e. the file system, into commands specific to the type of the flash chip present, i.e. the physical sector commands, by the standardized controller translating apparatus – not by the CPU as stated by the Applicant -- (e.g. see Col. 5, lines 30-35). The further limitation of “organize all mappings between a computer's memory and a flash array” upon which the Applicant relies is not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

With respect to (f), Ban clearly teaches about translating commands received from the CPU, i.e. the file system, into commands specific to the type of the flash chip present, i.e. the physical sector commands, by the standardized controller translating apparatus – not by the CPU as stated by the Applicant -- (e.g. see Col. 5, lines 30-35). Ban teaches that the flash abstraction logic (i.e. the group of interfaces/controllers, between the CPU and the flash memory medium) configured to map a logical sector status from the file system to a physical sector status of the flash memory medium (e.g.

Art Unit: 2186

see Col. 5, lines 30-35); and maintain memory requirements associated with operating the flash medium (e.g. see Col. 4, lines 33-39, 61-65).

### ***Conclusion***

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hetul Patel whose telephone number is 571-272-4184. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

*HBP*  
HBP

  
MATTHEW KIM  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER